Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A memory structure for use with a dual-speed Ethernet device, comprising:

an Address Resolution Table comprising a plurality of locations, each of said locations configured to store a packet destination address, wherein the Address Resolution Table is configured to

resolve addresses in a packet-based network switch, and

use a key to index one of said locations wherein the key is a predefined portion of the packet destination address associated with said indexed location via at least an offset in address space;

a Packet Storage Table configured to

receive a packet for storage in the packet-based network switch, and

share a preselected portion of memory with the Address Resolution Table;

and

a single buffer per packet mechanism configured to receive an individual packet, wherein the single buffer per packet mechanism is configured to perform only one transmit descriptor read per said individual packet and execute a first single access in order to locate the entire packet and a second single to access the packet destination address at the indexed location using the key, wherein the entire packet is to be transmitted,

wherein the memory structure implements memory arbitration for at least six types of memory accesses, and

wherein the memory structure facilitates full-duplex, non-blocked Ethernet switch operations at wire speeds.

2. (Previously Presented) The memory structure of claim 1, further comprising at least one of:

a Transmit Descriptor Table being associated with a corresponding packet-based network transmit port; and

a Free Buffer Pool comprising plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

3. (Previously Presented) The memory structure of claim 1 wherein the packet-based network switch implements an IEEE standard 802.3 communication protocol.

4. (Previously Presented) The memory structure of claim 3 wherein the switch comprises plural ports.

5. (Previously Presented) The memory structure of claim 4 wherein the switch comprises at least 8 ports.

6. (Previously Presented) The memory structure of claim 1 wherein an associative memory structure comprises one of an n-way associative memory, a hash table, a binary search structure, and a sequential search structure.

7. (Previously Presented) The memory structure of claim 3 wherein the number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

8. (Currently Amended) A memory structure comprising:

an Address Resolution Table comprising an associative memory structure comprising a plurality of locations, each of said locations configured to store a packet destination address, wherein the Address Resolution Table is configured to resolve addresses in a packet-based network switch and to use a key and an offset in address space to index one of said locations within the Address Resolution Table; and

a single buffer per packet mechanism configured to receive an individual packet, perform only one transmit descriptor read per said individual packet, and execute a first single access in order to locate the entire packet and a second single access to locate the packet destination address at the indexed location using the key, wherein the entire packet is to be transmitted, wherein the key comprises a predefined portion of a packet destination address,

wherein the memory structure implements a weighted priority, round-robin memory arbitration technique.

9. (Previously Presented) The memory structure of claim 8 further comprising a Packet Storage Table, the Packet Storage Table configured to receive at least one of a Packet Data address and a Packet Data Value.

10. (Previously Presented) The memory structure of claim 9 further comprising a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table configured to receive a Table Descriptor Address and a Table Descriptor Value.

11. (Previously Presented) The memory structure of claim 8 wherein the associative memory structure comprises one of a direct-mapped/one-way associative memory structure and a two-way associative memory structure.

12. (Previously Presented) The memory structure of claim 11 wherein the number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

13. (Currently Amended) A memory structure comprising a memory block, the memory block comprising:

an Address Resolution Table having comprising an associative memory structure comprising a plurality of locations, each of said locations configured to store a packet destination address, wherein the Address Resolution Table configured to resolve addresses in a packet-based network switch and to use a key to index one of said locations within the Address Resolution Table, wherein the key comprises a predefined portion of a packet destination address associated with the indexed location through at least an offset in address space;

a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table configured to receive a Table Descriptor Address and a Table Descriptor Value;

a Packet Storage Table, the Packet Storage Table configured to receive at least one of a Packet Data address portion and a Packet Data Value portion; and

a single buffer per packet mechanism configured to receive an individual packet, to perform only one transmit descriptor read per said individual packet, and to execute a first single access in order to locate the entire packet and a second single access to locate the packet destination address at the indexed location using the key, wherein the entire packet is to be transmitted,

wherein the memory structure implements a weighted priority, round-robin memory arbitration technique.

14. (Previously Presented) The memory structure of claim 13 wherein the associative memory structure comprises one of an n-way associative memory, a hash table, a binary search structure, and a sequential search structure.

15. (Previously Presented) The memory structure of claim 13 wherein the memory block comprises a shared memory block.

16. (Previously Presented) The memory structure of claim 13 wherein the Transmit Descriptor Table comprises a FIFO memory structure.

17. (Previously Presented) The memory structure of claim 16 wherein the FIFO memory structure comprises a circular FIFO memory structure, the FIFO memory structure comprising a head memory pointer and tail memory pointer.

18. (Previously Presented) The memory structure of claim 13 further comprising a Free Buffer Pool comprising plural memory buffers, each of the plural memory buffers comprising a pre-determined number of memory locations associated therewith.

19. (Previously Presented) The memory structure of claim 18, wherein the Free Buffer Pool further comprises a buffer control memory.

20. (Previously Presented) The memory structure of claim 19, wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the pre-determined number of buffer pool memory locations.

21. (Previously Presented) The memory structure of claim 18, wherein at least two of the Address Resolution Table, the Transmit Descriptor Table, the Packet Storage Table, and the Free Buffer Pool share a memory block.

22. (Previously Presented) The memory structure of claim 21 wherein a packet-based network switch implements an IEEE Standard 802.3 communication protocol and wherein a number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

23. (Previously Presented) The memory structure of claim 18, further comprising a free buffer manager, including:

a buffer bus controller;

a buffer bus register;

a buffer control finite state machine, operably coupled with the bus controller and the bus

register; and

a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

24. (Previously Presented) The memory structure of claim 23 wherein the buffer bus controller comprises:

a buffer free bus controller for detecting a buffer request and presenting the request to at least one of the finite state machine and the buffer search engine; and

a buffer grant bus controller for granting an available free buffer, as indicated by the buffer, as indicated by the buffer bus register.

25. (Previously Presented) The memory structure of claim 23 wherein the buffer search engine comprises a pipelined buffer search engine.

26. (Previously Presented) The memory structure of claim 23 wherein the buffer bus register comprises a LIFO.

27. (Previously Presented) The memory structure of claim 26 wherein the LIFO comprises an eight-location LIFO.

28. (Currently Amended) A packet-based switch comprising:

a shared memory structure comprising an Address Resolution Table and a Packet Storage Table, wherein the address resolution table comprises a plurality of locations, each of said locations configured to store a packet destination address;

a key and an offset in address space to index one of said locations within the Address Resolution Table; and

a single buffer per packet mechanism configured to receive an individual packet, perform only one transmit descriptor read per said individual packet, and execute a first single access in order to locate the packet destination address at the indexed location using the key, wherein the key is a predefined portion of the packet destination address at the indexed location, and a second single access to locate the entire packet, wherein the entire packet is to be transmitted,

wherein the packet-based switch performs full-duplex, non-blocked Ethernet switch operations at wire speed.

29. (Previously Presented) The packet-based switch of claim 28 wherein the switch implements an IEEE Standard 802.3 communication protocol.

30. (Previously Presented) The packet-based switch of claim 29 wherein the switch comprises plural ports.

31. (Previously Presented) The packet-based switch of claim 28 wherein the number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

32. (Currently Amended) A packet-based switch comprising a memory structure, the memory structure comprising:

an Address Resolution Table comprising an associative memory structure, the Address

Resolution Table comprising a plurality of locations, each of said locations configured to store a packet destination address, wherein the Address Resolution Table is configured to resolve addresses in a packet-based network switch and use a key to index one of said locations using at least an offset in address space wherein the key comprises a predefined portion of the packet destination address at the indexed location;

a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table configured to receive a Table Descriptor Address and a Table Descriptor Value;

a Packet Storage Table, the Packet Storage Table configured to receive at least one of each of a Packet Data address portion and a Packet Data Value portion; and

a single buffer per packet mechanism configured to receive an individual packet, perform only one transmit descriptor read per said individual packet, and execute a first single access in order to locate the entire packet and a second single access to locate the packet destination address at the indexed location using the key, wherein the entire packet is to be transmitted,

wherein the memory structure facilitates full-duplex, non-blocked Ethernet switch operations at wire speed.

33. (Previously Presented) The packet-based switch of claim 32, wherein the associative memory structure comprises one of an n-way associative memory, a hash table, a binary search structure, and a sequential search structure.

34. (Previously Presented) The packet-based switch of claim 32, wherein the memory structure comprises a memory block, and wherein the memory block comprises a shared memory block.

35. (Previously Presented) The packet-based switch of claim 32 wherein the Transmit

Descriptor Table comprises a FIFO memory structure.

36. (Previously Presented) The packet-based switch of claim 35 wherein the FIFO memory structure comprises a circular FIFO memory structure the FIFO memory structure comprising a head memory pointer and a tail memory pointer.

37. (Previously Presented) The packet-based switch of claim 32 further comprising a Free Buffer Pool comprising plural memory buffers, each of the plural memory buffers comprising a pre-determined number of memory locations associated therewith.

38. (Previously Presented) The packet-based switch of claim 37, wherein the Free Buffer Pool further comprises a buffer control memory.

39. (Previously Presented) The packet-based switch of claim 38, wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the predetermined number of buffer pool memory locations.

40. (Previously Presented) The packet-based switch of claim 37, wherein at least two of the Address Resolution Table, the Transmit Descriptor Table, the Packet Storage Table, and the Free Buffer Pool share a memory block.

41. (Previously Presented) The packet-based switch of claim 34 wherein a packet-based network switch implements an IEEE Standard 802.3 communication protocol and wherein a number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and'

one cycle per eight bytes for a frame data write.

42. (Previously Presented) The packet-based switch of claim 38, further comprising a free buffer manager, including:

a buffer bus controller;

a buffer bus register;

a buffer control finite state machine, operably coupled with the bus controller and the bus register; and

a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

43. (Previously Presented) The packet-based switch of claim 42 wherein the buffer bus controller comprises:

a buffer free bus controller for detecting a buffer request and present the request to at least one of the finite state machine and the buffer search engine; and

a buffer grant bus controller for granting an unavailable free buffer, as indicated by the buffer bus register.

44. (Previously Presented) The packet-based switch of claim 42 wherein the buffer search engine comprises a pipelined buffer search engine.

45. (Previously Presented) The packet-based switch of claim 42 wherein the buffer bus register comprises a LIFO.

46. (Previously Presented) The packet-based switch of claim 45 wherein the LIFO comprises an eight-location LIFO.

47. (Previously Presented) The packet-based switch of claim 33 wherein the switch implements an IEEE Standard 802.3 communication protocol.

48. (Previously Presented) The packet-based switch of claim 47 wherein the switch comprises plural ports.

49. (Previously Presented) The packet-based switch of claim 47 wherein the switch comprises at least 4 ports.

50. (Previously Presented) The packet-based switch of claim 47 wherein the switch comprises at least 8 ports.

51. (Previously Presented) The packet-based switch of claim 45 wherein a packet-based network switch implements an IEEE Standard 802.3 communication protocol and wherein a number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

52. (Currently Amended) A packet-based switch comprising an Address Resolution Table comprising a one-way associative memory structure comprising a plurality of locations, each of said locations configured to store a packet destination address, wherein the Address Resolution Table is configured to use a key to index a one of said locations within the Address Resolution Table using at least an offset in address space, and a Packet Data Buffer Table configured to share a memory block with an Address Resolution Table, and a single buffer per packet mechanism configured to receive an individual packet, to perform only one transmit descriptor read per said individual packet, and of to execute a first single access in order to locate an entire packet and a second single access to locate the packet destination address at the indexed location using the key, wherein the key is a predefined portion of the located packet destination address, wherein the entire packet is to be transmitted, wherein the packet-based switch performs full-duplex, non-blocked Ethernet switch operations at wire speed.

53 (Previously Presented) The packet-based switch of claim 52 wherein the switch comprises plural ports.

54. (Previously Presented) The packet-based switch of claim 52 wherein the switch comprises at least 4 ports.

55. (Previously Presented) The packet-based switch of claim 52 wherein the switch comprises at least 8 ports.

56. (Previously Presented) The packet-based switch of claim 52 wherein a packet-based network switch implements an IEEE Standard 802.3 communication protocol and wherein a number of memory accesses required per Ethernet frame is one of:

one cycle per frame for address resolution;

one cycle per frame for address learning;

one cycle per frame for transmission read;

one cycle per frame for transmission write;

one cycle per eight bytes for a frame data read; and

one cycle per eight bytes for a frame data write.

57. (Currently Amended) A packet-based switch, comprising;

an Address Resolution Table comprising a direct-mapped/one-way associative memory structure comprising a plurality of locations, each of said locations configured to store a packet destination address, wherein the Address Resolution Table is configured to resolve addresses in a packet-based network switch, and to use a key and an offset in address space to index a one of said locations; and

a single buffer per packet mechanism configured to receive an individual packet, to perform only one transmit descriptor read per said individual packet, and to execute a first single access in order to locate an entire packet and a second single access to locate the packet destination address at the indexed location using the key, wherein the key is a predefined portion of the located packet destination address, wherein the entire packet is to be transmitted,

wherein the packet-based switch makes a transmit descriptor request during a transmission of a previous frame, and

wherein the packet-based switch facilitates full-duplex, non-blocked Ethernet switch operations at wire speed.

58. (Previously Presented) The packet-based switch of claim 57 wherein the direct-mapped/one-way associative memory is searched using a destination address key direct-mapped address search.

59. (Previously Presented) The packet-based switch of claim 58 wherein the switch implements an IEEE Standard 802.3 communication protocol.

60. (Previously Presented) The packet-based switch of claim 59, wherein the switch comprises plural ports.